# LDPC Decoder

The LDPC Decoder is composed of a Xilinx Vivado project, LDPC\_Dual, that uses the Block Diagram feature to integrate five Xilinx HLS modules that have been written in C++ and have generated RTL blocks. The files are shown in Figure 1.



Figure 1 Decoder Projects

The HLS project provide the following functions:

* LDPC\_CTRL – configures parameters needed to perform decoding of multiple LDPC Block codes. The codes supported by this design are: Block Sizes 1024 & 4096; Block Rates ½, 2/3 & 4/5.
* LDPC\_data\_buffer\_mult – receives data from the SOQPSK demodulator and places them in the Raw Data buffers. These will be used by the decoder block. There are two banks of Raw Data buffers, one for Decoder A & one for Decoder B. Each data buffer bank multiple BRAMs. Data will be distributed between the rams differently depending on the Block Size & Rate being decoded.
* LDPC\_Decoder3U – This block performs the LDPC decoding based on the Min-Sum algorithm described in the reference documents in the reference folder. The LDPC\_Dual project uses two decoders to increase the amount of processing time available to support codes rate greater than 20 Mbps.
* LDPC\_Out – Similar to the input buffer, there are two Decoded data buffers that have multiple BRAMS. This module facilitates the output of the decoded data back to the demod.
* LDPC\_CLK\_DIV – This module generates an output write clock that is at a reduced rate to compensate for the removal of the ASM and Parity bits.

The simplified block diagram for the LDPC\_Dual decoder project is shown in Figure 2.



Figure 2 LDPC\_Dual Simplified Block Diagram

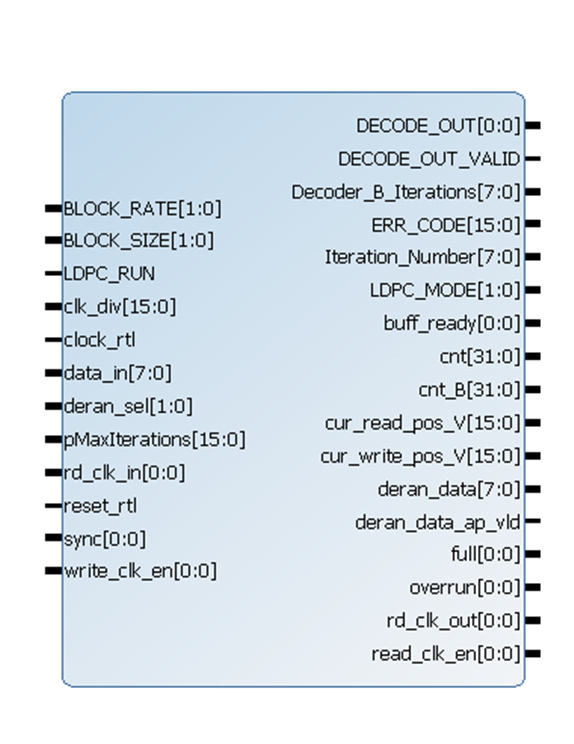
The I/O for the decoder is shown in Figure 3 with Inputs on the left side and outputs on the right side. 

Figure 3 LDPC\_Dual Inputs/Outputs

## Inputs

The following table provides information on the input parameters for the decoder.

| Parameter | Valid Values | Description |
| --- | --- | --- |
| BLOCK\_RATE | 1 – Rate ½  2 – Rate 2/3  3 – Rate 4/5 | Sets the code rate for the input Block |
| BLOCK\_SIZE | 1 – 1024  2 – 4096 | The uncoded data block size |
| LDPC\_RUN | 1 – Run  0 – Idle | Enables the operation of the LDPC\_Decoder |
| Clk\_div | 1 - 65535 | Sets the number of clock inputs required to produce a rd\_clk\_out pulse. Used to set the decoder output bit rate. |
| Clock\_rtl | Nominal 93.33333 MHz | The master clock for the decoder |
| Data\_in | 127 to -127 | 2’s compliment soft decision data from demodulator |
| Deran\_sel | 0 – None  1 – CCSDS  2 – IRIG (not used) | IRIG is no longer used because it operates on the entire codeblock. IRIG derandomization is achieved by passing the decoder output through the standard demod derandomizer. |
| pMaxIterations | 1 to 50 | Sets the maximum number of iterations attempted before exiting the decoder. This affects the maximum bit rate supported by the decoder. A higher number will lower the maximum bit rate. If a successful decode is not achieved by the maximum number the current decoded data (with errors) is transferred to the decoded data buffer |
| Rd\_clk\_in |  | On the asserted level, the next data bit from the decoded data buffer is output from the madule. This signal acts like a clock enable. |
| Reset\_rtl | Active High | Resets the module to its power-up state. |
| Sync | 1 – Codeblock data is present  0 – ASM data is present | The ASM state is used to synchronize blocks in the decoder and to determine when to “ping-pong” between the two decoders/BRAMs |
| Write\_clk\_en | Active High | Indicates that valid data is on the Data\_in port. |

## Outputs

The following table provides information on the output parameters of the decoder.

| Parameter | Valid Values | Description |
| --- | --- | --- |
| DECODE\_OUT | N/A | The next data bit from the decoded data buffer |
| DECODE\_OUT\_VALID | 1 – Valid data | An enable for the DECODE\_OUT |
| Decoder\_B\_iterations | 0 – 256 | The number of iterations required for the last decode |
| ERR\_Code | N/A | This output is not used |
| Iteration\_Number | 0 – 256 | Ther number of iterations for the last decode for decoder A |
| LDPC\_MODE | 1 – Operational  0 – Idle | Indicates the operating state of the decoder |
| Buff\_ready | 1 – Ready for Data | Data can be written to the device |
| Cnt | N/A | Debugging output for decoder A |
| Cnt\_B | N/A | Debugging output for decoder B |
| Cur\_read\_pos\_V | 0 – 10240 | Indicates the current decoded data buffer position |
| Cur\_write\_pos\_V | 0 – 10240 | Indicates the current raw data buffer position |
| Deran\_data | -127 – 127 | Pre-decoded derandomized codeblock data. Only used for debugging. |
| Deran\_data\_ad\_bld |  | Active when valid deran data is present |
| Full | N/A | Debugging |
| Overrun | N/A | debugging |
| Rd\_clk\_out |  | The divided clock output sent to the demod to indicate the next bit can be clocked. |
| Read\_clk\_en |  | Active when the Rd\_clk\_out signal is valid. |